

Handwritten: extending in the first direction.

IV. In the Drawings

Please amend the drawings per the handwritten changes in red ink. Upon approval thereof, formal drawings reflecting these changes will be submitted.

V. In the Title of the Invention

Please amend the title to: SMART CARD AND CIRCUITRY LAYOUT THEREOF FOR REDUCING CROSS-TALK

Remarks

Status of the Claims

Upon entry of the present amendment, claims 1, 4-6 and 8-23 are pending in the present application. Claims 21-23 are newly added, and claims 1, 8, 14 and 21 are the independent claims.

Allowable Subject Matter

Applicant gratefully acknowledges the indication by the Examiner of the allowability of the subject matter of dependent claims 2, 4, 5, 15, 16 and 18-20. Applicant also gratefully acknowledges indication by the Examiner of the subject matter of claims 7, 8 and 14 subject to Applicant's overcoming the rejection thereof under 35 USC § 112 ¶ 2. As discussed below, all claims are believed to be in condition for allowance.

Amendments to the Claims

Claim 1 has been amended to include the allowable subject matter of claim 2.

As such this claim is believed to be in condition for allowance. Moreover, claims 4, 5 and 6, which depend from claim 1 are also believed to be allowable. Allowance of these claims is earnestly solicited.

Claims 8 and 14 have been amended to correct the grammatical errors indicated in the objections thereto, as well as the rejection due to lack of proper antecedent basis thereto. As such, these claims are believed to be allowable. Allowance is earnestly solicited.

Claims 3, 7, 10, 14, 17 and 9-13 were rejected under 35 USC USC § 112 ¶ 2 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The term 'as many times as possible' was the problematic element of the claims. Claims 8, 10, 14 and 17 have been amended to include the element 'two or more times' in reference to the number of times the conductive line passes across the bit lines. This is believed to suitably clarify these claims, thereby nullifying this rejection. Moreover, basis for the this amendment may be found in the application as filed, for example, via a review of Fig. 3. As such, it is respectfully submitted that these amendments add no new matter.

Newly Added Claims

Newly added claims 21-23 are submitted for examination.

Amendments to the Specification and Abstract of the Disclosure

Applicant's attorney gratefully acknowledges the Examiner's pointing out of errors in the specification and abstract. The amendments thereto are believed to correct these errors.

Conclusion

For at least the reasons set forth above withdrawal of all objections and rejections is respectfully requested. An early notice of all pending claims is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

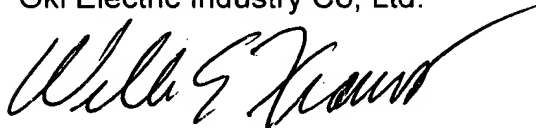
Except as otherwise stated in the previous Remarks, applicants note that each of the amendments have been made to place the claims in better form for U.S. practice or to clarify the meaning of the claims; not to distinguish the claims from prior art references, otherwise narrow the scope or comply with other statutory requirements. Moreover, Applicants reserve all rights they may have under the Doctrine of Equivalents.

A petition for a one-month extension of time under 37 C.F.R. §1.136(a) is hereby made. Permission is given to charge the fee for this extension of time under 37 C.F.R. §1.17 to Deposit Account Number 50-0238. Moreover, the fees for additional claims may also be charged to this Deposit Account.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:

Oki Electric Industry Co, Ltd.

A handwritten signature in black ink, appearing to read 'William S. Francos', with a long, sweeping horizontal line extending to the right.

William S. Francos, Esq.

Reg. No. 38,456

Date: December 30, 2002

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Marked Version Showing Changes to Claims

1. (Once Amended) A semiconductor integrated circuit, comprising:

a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer,

wherein the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines, and is shaped to be a step form having a part extending in the first direction.

8. (Once Amended) A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of a component in the ROM; and

a RAM, which enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines.

10. (Once Amended) A smart card according to claim 8, wherein

the conductive line is shaped so as to pass across the bit lines [as many as possible] two or more times.

14. (Once Amended) A smart card, comprising:

a ROM;

a CPU using a runnable program fixed at the time of the manufacture of a component in the ROM; and

a RAM, which enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, wherein the conductive line is shaped to be a step form partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines [as many as possible] two or more times.

17. (Once Amended) A method according to claim 15, wherein

the conductive line is shaped so as to pass across the bit lines [as many as possible] two or more times.

**Marked Version Showing Changes to Specification, the Abstract of the Disclosure
and the Title of the Invention**

Paragraph on page 1, line 1:

The present invention relates to [a] small size cards, such as smart cards and chip cards; and more particularly, to a design of conductive lines arranged over bit lines of a ROM block.

Paragraph on page 6, line 8:

Fig. 3 is a circuitry layout 102 in a smart card according to a first embodiment of the present invention. A ROM includes bit lines 104 arranged to extend in a first direction, which is a vertical in the figure. The bit lines 104 are formed in a first layer. In a second layer located above the first layer, conductive lines 106 are formed to extend in a second direction, which is orthogonal to the first direction. Each of the conductive lines 106 is shaped to be a step form so as to across the bit lines 104 as [many times] much as possible and to improve the degree of freedom of circuitry design. In other words, the conductive lines 106 can extend in any direction[s] at the ends, so that the semiconductor integrated circuit can be designed without a lot of restrictions.

Paragraph on page 7, line 12:

Fig. 4 is another circuitry layout in a smart card according to a second embodiment of the present invention. A ROM includes bit lines 204 arranged to extend

in a first direction, which is a vertical in the figure. The bit lines 204 are formed in a first layer. In a second layer located above the first layer, conductive lines 206 are formed to extend in a second direction, which is orthogonal to the first direction. Each of the conductive lines 206 is shaped to be a step form so as to across the bit lines 204 as [many] much as possible and to improve the degree of freedom of circuitry design. In other words, the conductive lines 206 can extend any directions at the ends, so that the semiconductor integrated circuit can be designed without a lot of restrictions.

Abstract

A semiconductor integrated circuit includes a ROM having bit lines extending in a first direction in a first layer[; and a]. A conductive line is arranged in a second layer above the first layer, extending in a second direction, which is orthogonal to the first direction, across the bit lines. The conductive line is shaped to be a step form having a part extending in the first direction.

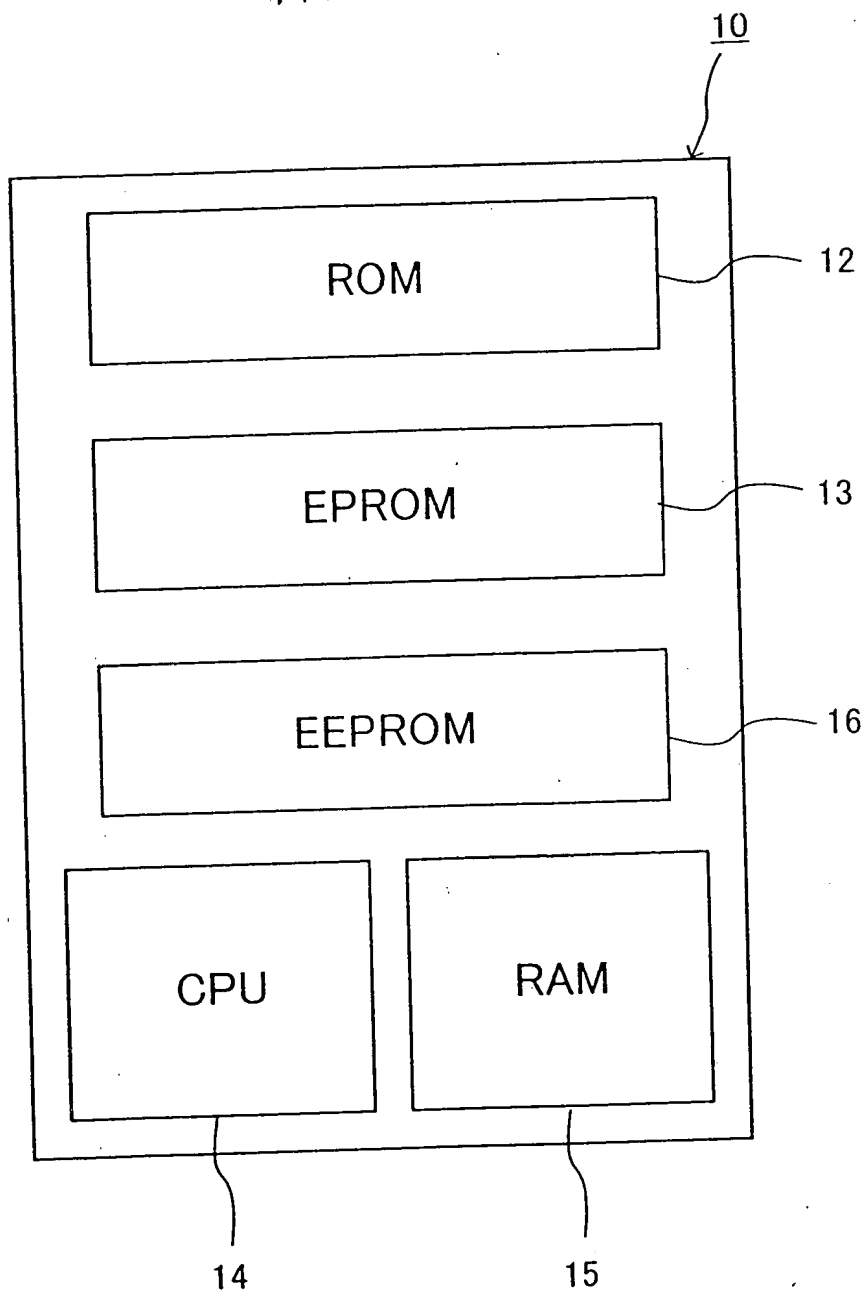
Title

SMART CARD AND CIRCUITRY LAYOUT THEREOF FOR REDUCING CROSS-TALK



Proposed Changes to Fig. 1

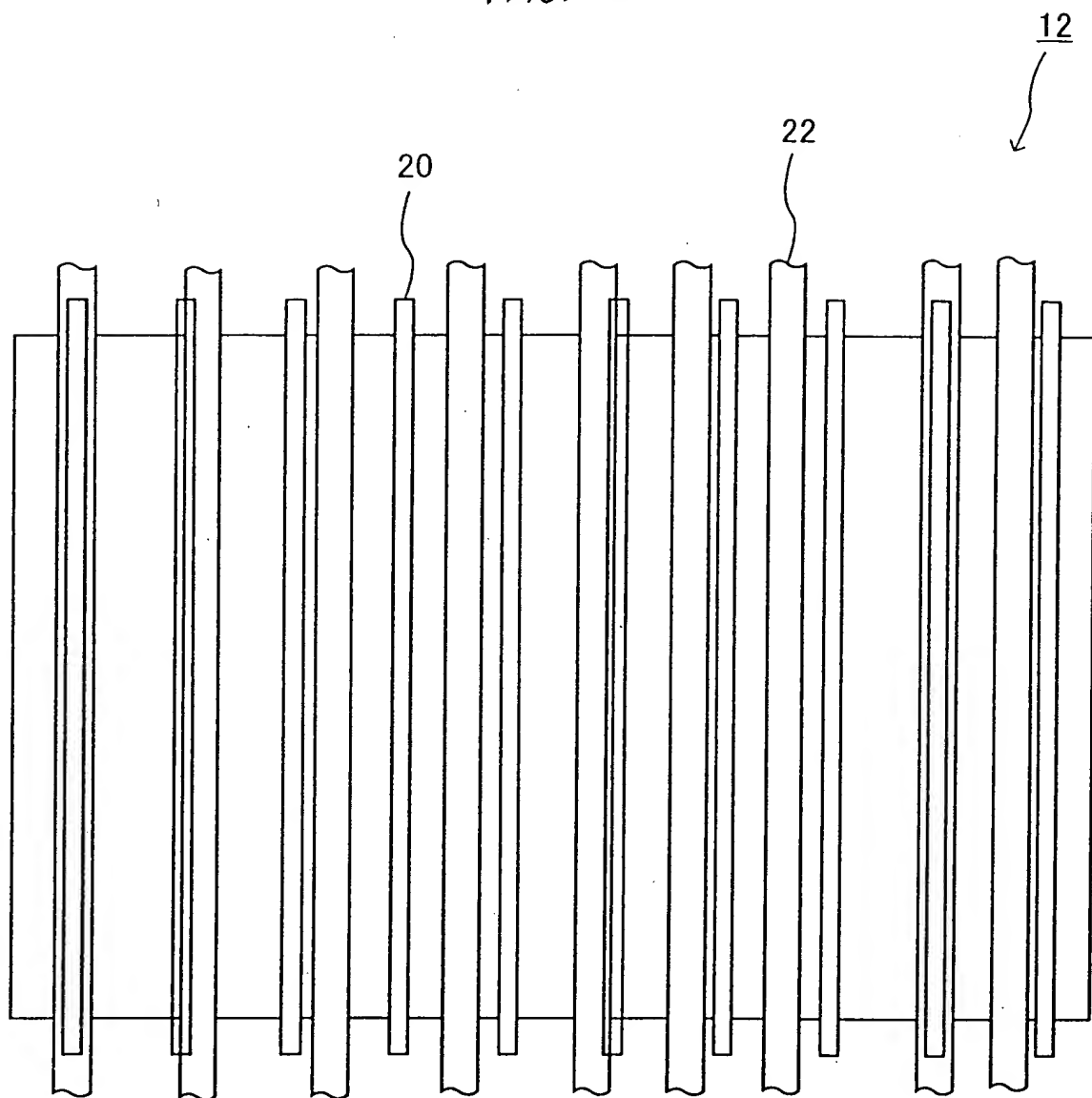
FIG. 1
Prior Art



3026 3040 3040 3040

Proposed Changes to Fig. 2

FIG. 2
Prior Art



Approved
[Signature]